For example, the second conductive type impurity amount of the utmost inner periphery region becomes excess. Thus, when the device turns off, the depletion layer proceeds from the center region to the periphery region so that the withstand voltage of the device is improved. Specifically, the reduction of the withstand voltage is limited to the withstand voltage of the periphery region as the upper limit. Thus, the device has high withstand voltage.

[0010] Further, the difference of the impurity amount of the utmost outer periphery pair in the periphery region is smaller than the maximum difference of the impurity amount of another pair in the periphery region. This utmost outer periphery pair is disposed at a portion, at which the electric filed is easily concentrated. Thus, even when the impurity amount of the first region and the second region in the periphery region is deviated in the manufacturing process, the concentration of the electric filed is relaxed. Thus, the withstand voltage of the device is improved.

[0011] Accordingly, the withstand voltage of the device having the SJ structure is improved, even when the impurity amount is deviated in the manufacturing process. Further, the method for manufacturing the SJ structure is easily performed. Thus, the yielding ratio of product is improved.

[0012] Further, a method for manufacturing a semiconductor device is provided. The device includes a semiconductor layer having a first column and a second column. The first column has a first conductive type and the second column has a second conductive type. The first and the second columns extend in a thickness direction of the device. The first and the second columns are repeated alternately in a plane perpendicular to the thickness direction. The method includes the steps of: forming a mask on a semiconductor wafer having the first conductive type, wherein the mask includes a center region mask, an inner periphery region mask and an outer periphery region mask, wherein the center region mask has a plurality of openings, each distance of which is constant, wherein the inner periphery region mask has a plurality of openings, each distance of which is smaller than the distance of the openings of the center region mask, wherein the outer periphery region mask has a plurality of openings, each distance of which is larger than the distance of the openings of the inner periphery region mask; forming a plurality of trenches on the semiconductor wafer through the openings of the mask by an anisotropic etching method; and forming a semiconductor region having the second conductive type in each trench.

[0013] The method provides the semiconductor device having the SJ structure. The withstand voltage of the device having the SJ structure is improved, even when the impurity amount is deviated in the manufacturing process. Further, the method for manufacturing the SJ structure is easily performed. Thus, the yielding ratio of product is improved.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] The above and other objects, features and advantages of the present invention will become more apparent from the following detailed description made with reference to the accompanying drawings. In the drawings:

[0015] **FIG. 1** is a partial cross sectional view showing a semiconductor device according to a first embodiment of the present invention;

[0016] **FIG. 2** is a partial plan view showing the device according to the first embodiment;

[0017] **FIG. 3** is a graph showing a relationship between a position and excess P type impurity amount, according to the first embodiment;

[0018] **FIG. 4** is a graph showing a relationship between a deviation of the impurity concentration and a withstand voltage, according to the first embodiment;

[0019] **FIG. 5** is a cross sectional view showing electric potential distribution in a periphery region of the device, according to the first embodiment;

[0020] **FIG. 6** is a cross sectional view showing electric potential distribution in a periphery region of a comparison device;

[0021] **FIG. 7** is a cross sectional view explaining a method for manufacturing a drift layer, according to the first embodiment;

[0022] **FIG. 8** is a cross sectional view explaining the method for manufacturing the drift layer, according to the first embodiment;

[0023] **FIG. 9** is a cross sectional view explaining the method for manufacturing the drift layer, according to the first embodiment;

[0024] **FIG. 10** is a cross sectional view explaining the method for manufacturing the drift layer, according to the first embodiment;

[0025] **FIG. 11** is a cross sectional view explaining the method for manufacturing the drift layer, according to the first embodiment; and

[0026] **FIG. 12** is a partial plan view showing a semiconductor device according to a second embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

First Embodiment

[0027] A semiconductor device having a super junction (i.e., SJ) structure according to a first embodiment of the present invention is shown in **FIGS. 1 and 2**. **FIG. 1** is a partial cross sectional view showing a center region **12** and a periphery region **14** of the device. **FIG. 2** is a partial plan view showing the device corresponding to line II-II in **FIG. 1**. Here, **FIG. 1** shows the device taken along line I-I in **FIG. 2**. Specifically, **FIG. 2** shows a main part of the device represents, specifically, a corner of the device.

[0028] The device is mainly made of silicon-based semiconductor. However, the device can be made of another semiconductor material.

[0029] As shown in **FIG. 1**, the center region **12** includes a semiconductor switching device, and the periphery region **14** is disposed around the center region **12**. In this device, the switching device is formed of a MOSFET. Specifically, the device includes a N^+ conductive type (i.e., N^+) drain layer **24**, a drift layer **26** as an example of a semiconductor layer, and a P conductive type (i.e., P) body layer **28**, which are stacked in this order. Thus, the device has a stacked structure. This structure is formed from the center region **12** to the